



PJM35P40TES

P-Channel Enhancement Mode Power MOSFET

Product Summary

- $V_{DS} = -40V, I_D = -48A$
- $R_{DS(on)} < 15m\Omega @ V_{GS} = -10V$
- $R_{DS(on)} < 19m\Omega @ V_{GS} = -4.5V$

Features

- Advanced Trench Technology
- 100% Avalanche Tested
- 100% DVDS
- RoHS Compliant
- Halogen and Antimony Free
- Moisture Sensitivity Level 3
- Molding Compound Meets UL 94 V-0 Flammability Rating

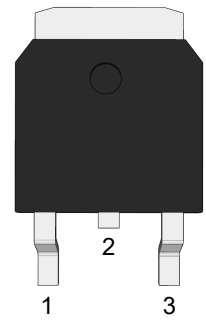
Application

- Load Switch
- PWM Application
- Power Management

Marking Code



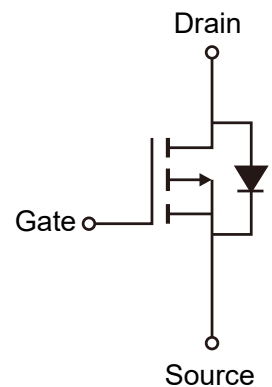
TO-252S



(Top View)

Pin	Description
1	Gate
2	Drain
3	Source

Schematic Diagram



Absolute Maximum Ratings

Ratings at 25°C case temperature unless otherwise specified.

Parameter		Symbol	Value	Unit
Drain-Source Voltage		$-V_{DS}$	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current-Continuous	$T_C = 25^\circ C$	$-I_D$	48	A
	$T_C = 100^\circ C$		29	
Drain Current-Pulsed ^{Note1}		$-I_{DM}$	192	A
Single Pulse Avalanche Energy ^{Note2}		E_{AS}	90	mJ
Maximum Power Dissipation		P_D	55	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Thermal Characteristics

Thermal Resistance, Junction-to-Ambient ^{Note3}	$R_{\theta JA}$	45	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.3	°C/W



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Electrical Characteristics

(T_J=25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	-V _{(BR)DSS}	V _{GS} =0V, I _D =-250μA	40	--	--	V
Zero Gate Voltage Drain Current	-I _{DSS}	V _{DS} =-40V, V _{GS} =0V	--	--	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage ^{Note4}	-V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	1	1.6	2.5	V
Drain-Source On-Resistance ^{Note4}	R _{DS(on)}	V _{GS} =-10V, I _D =-20A	--	11.5	15	mΩ
		V _{GS} =-4.5V, I _D =-10A	--	14.5	19	mΩ
Forward Transconductance ^{Note4}	g _{FS}	V _{DS} =-5V, I _D =-2A	--	10.5	--	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =-20V, V _{GS} =0V, f=1MHz	--	2056	--	pF
Output Capacitance	C _{oss}		--	212	--	pF
Reverse Transfer Capacitance	C _{rss}		--	159	--	pF
Gate resistance	R _g	V _{DS} =0V, V _{GS} =0V, f=1MHz	--	15	--	Ω
Total Gate Charge	Q _g	V _{DS} =-20V, I _D =-10A, V _{GS} =-10V	--	33	--	nC
Gate-Source Charge	Q _{gs}		--	6	--	nC
Gate-Drain Charge	Q _{gd}		--	7	--	nC
Switching Characteristics						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-20V, I _D =-10A, V _{GS} =-10V, R _{GEN} =2.5Ω	--	9.5	--	nS
Turn-on Rise Time	t _r		--	19.4	--	nS
Turn-off Delay Time	t _{d(off)}		--	50	--	nS
Turn-off Fall Time	t _f		--	26	--	nS
Source-Drain Diode Characteristics						
Diode Forward Voltage ^{Note4}	-V _{SD}	V _{GS} =0V, I _S =-15A	--	--	1.2	V
Diode Forward Current	-I _S		--	--	48	A
Reverse Recovery Time	trr	I _F =-10A, di/dt=100A/μS	--	30	--	nS
Reverse Recovery Charge	Qrr		--	38	--	nC

Note:

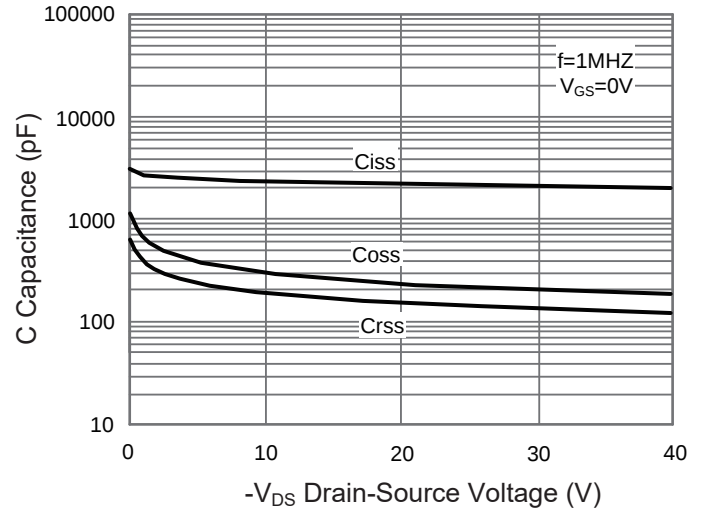
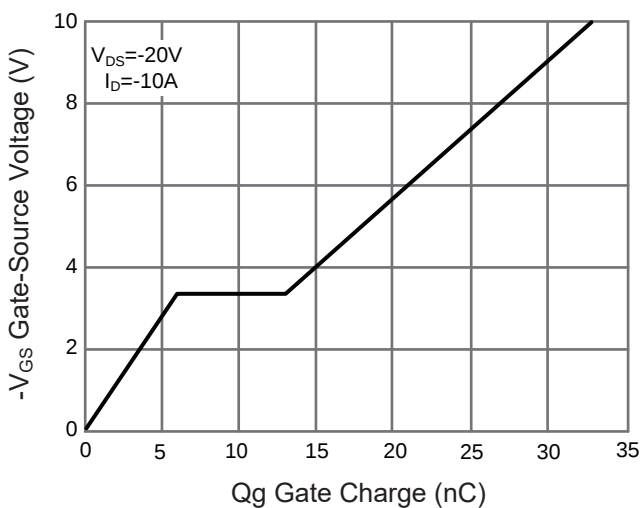
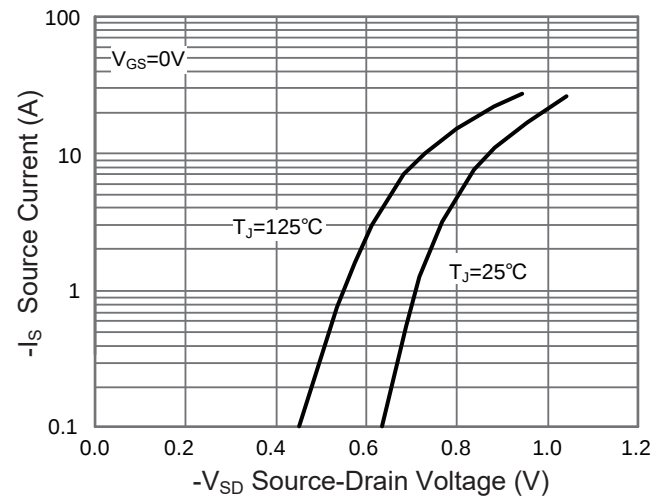
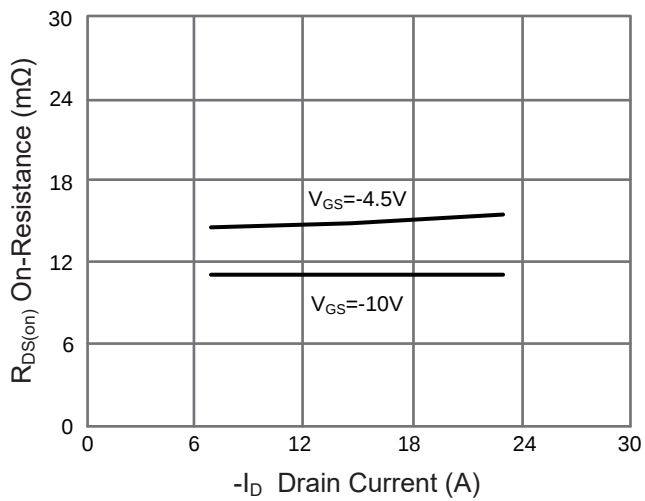
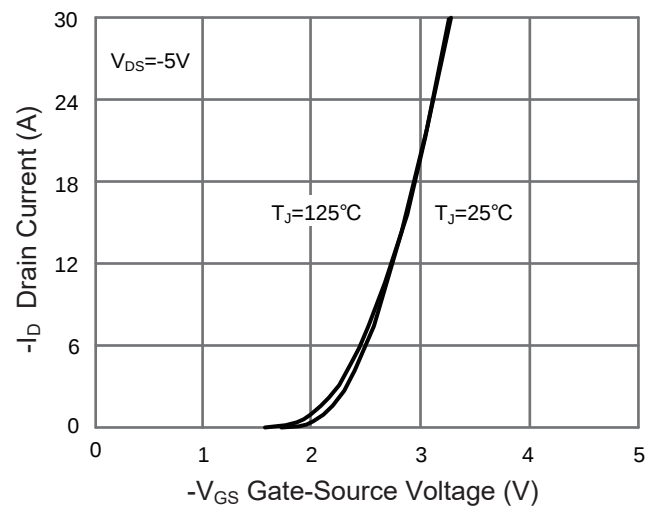
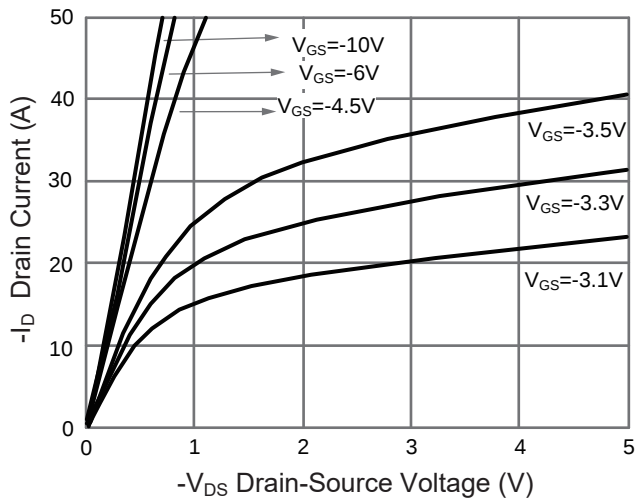
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. E_{AS} condition: T_J=25°C, V_{DD}=-20V, V_G=-10V, R_G=25Ω, L=0.5mH, I_{AS}=-19A
3. Surface mounted on 1inch² FR-4 board with 2OZ copper
4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%



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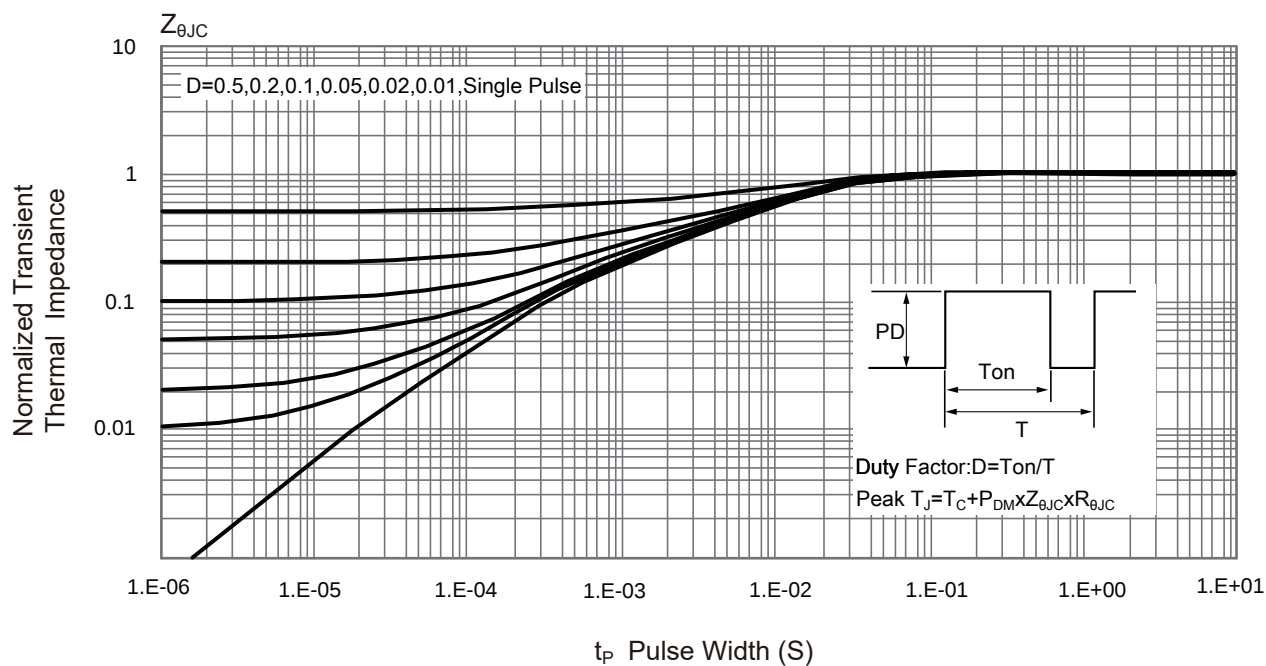
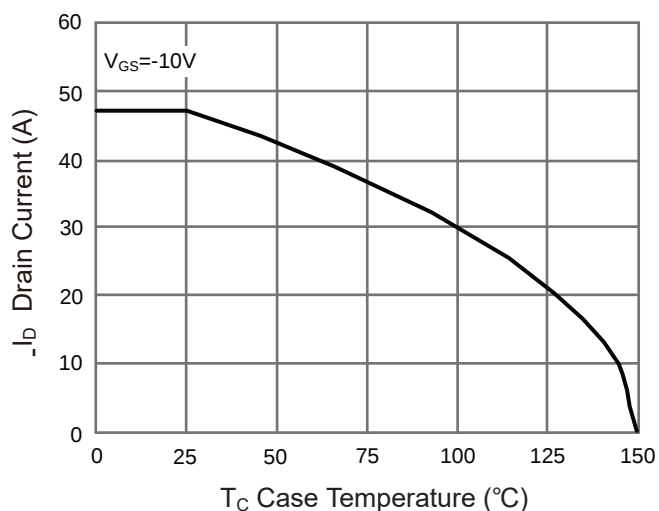
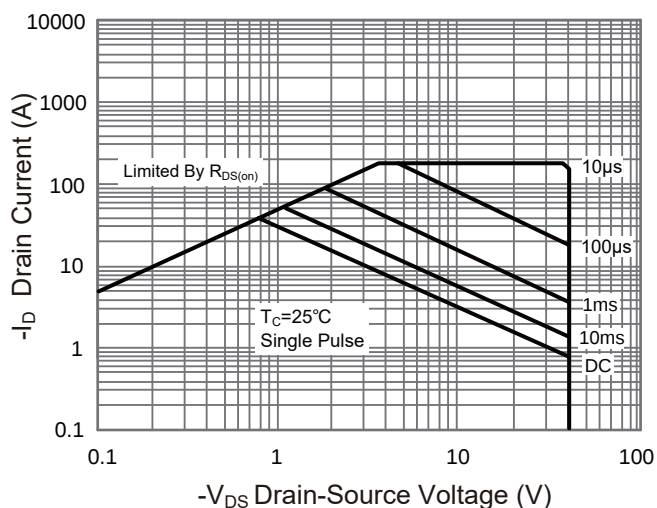
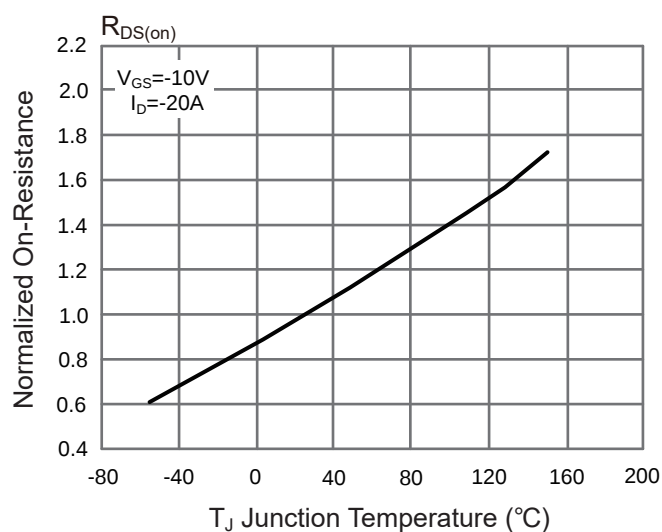
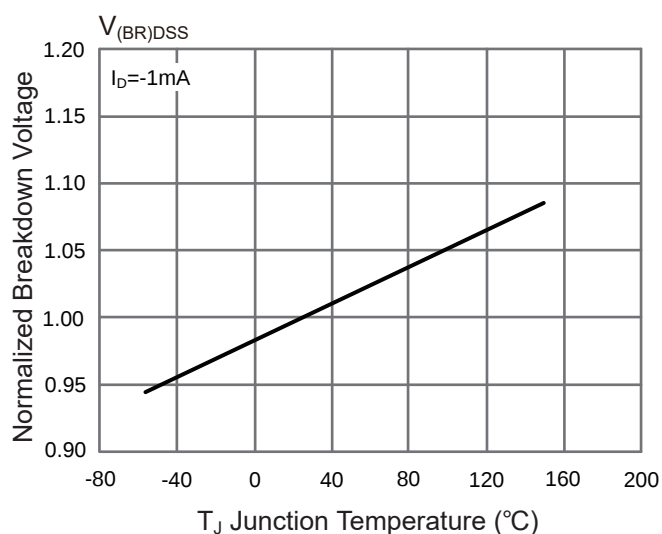
Typical Characteristic Curves





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Test Circuit

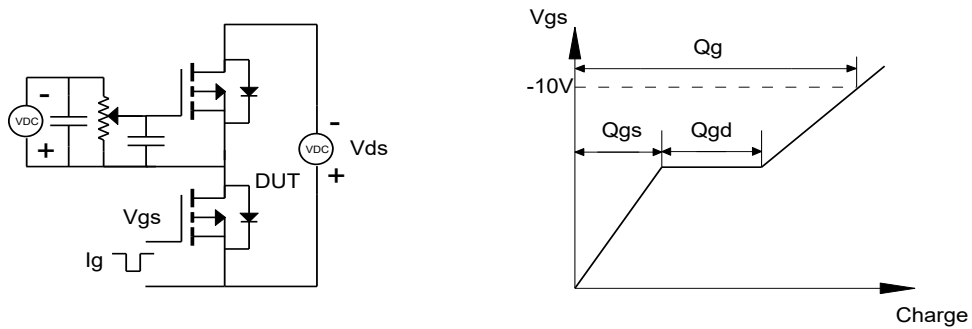


Figure 1: Gate Charge Test Circuit & Waveform

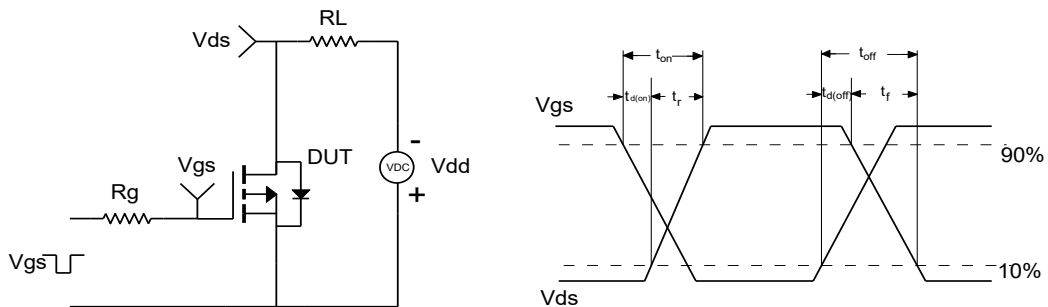


Figure 2: Resistive Switching Test Circuit & Waveform

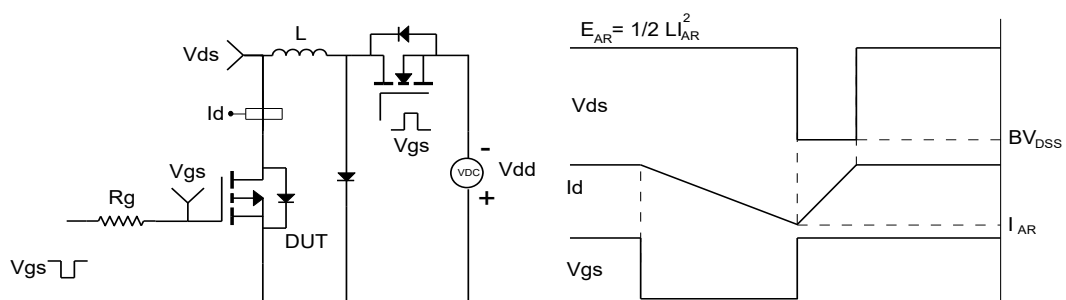


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

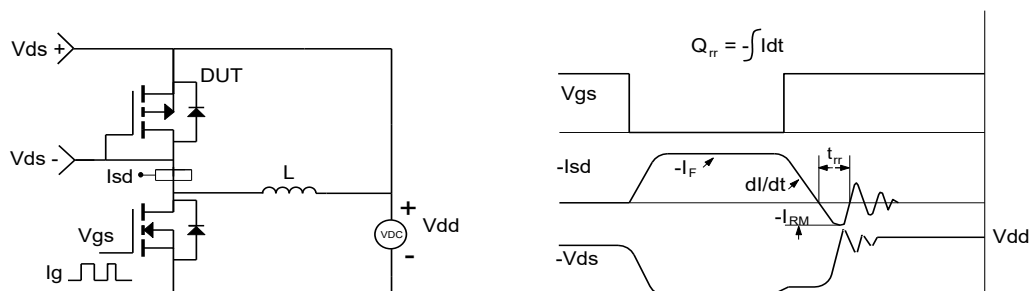


Figure 4: Diode Recovery Test Circuit & Waveform



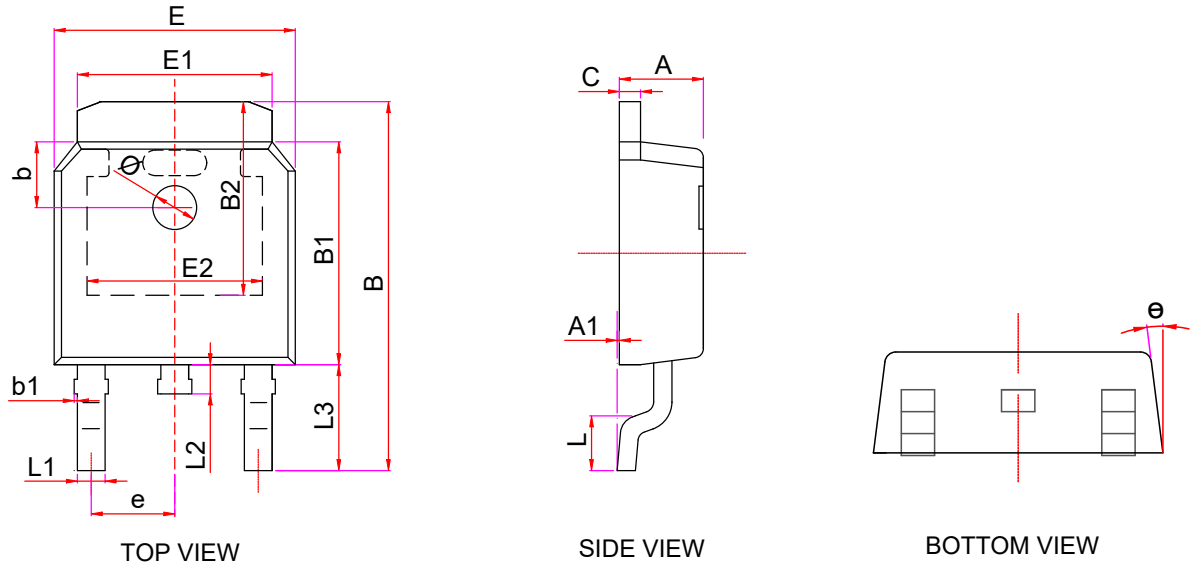
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Package Outline

TO-252S

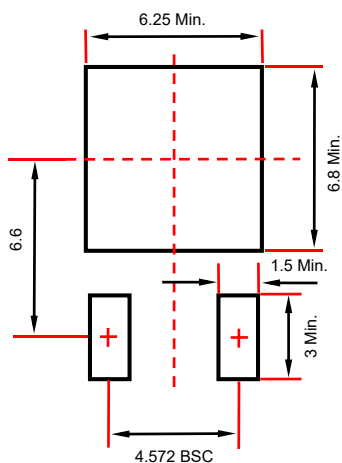
Dimensions in mm



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	2.200	2.300	2.400	0.087	0.090	0.094
A1	0.000	-	0.130	0.000	-	0.005
Ø	1.100	1.200	1.300	0.043	0.047	0.051
C	0.400	0.500	0.600	0.016	0.020	0.024
L	1.550	1.650	1.750	0.061	0.065	0.069
E	6.500	6.600	6.700	0.256	0.260	0.264
E1	5.200	5.300	5.400	0.205	0.209	0.213
E2	4.650	4.800	4.950	0.183	0.189	0.195
B	9.900	10.100	10.300	0.390	0.398	0.406
B1	5.800	6.000	6.200	0.228	0.236	0.244
B2	5.100	5.250	5.400	0.200	0.207	0.213
b	1.500	1.600	1.700	0.059	0.063	0.067
b1	0.100MAX			0.0039MAX		
L1	0.600	0.700	0.800	0.024	0.028	0.032
L2	0.700	0.800	0.900	0.028	0.032	0.036
L3	3.000	3.100	3.200	0.118	0.122	0.126
e	2.230	2.280	2.330	0.088	0.090	0.092
θ	9°			9°		

Suggested Pad Layout

TO-252S



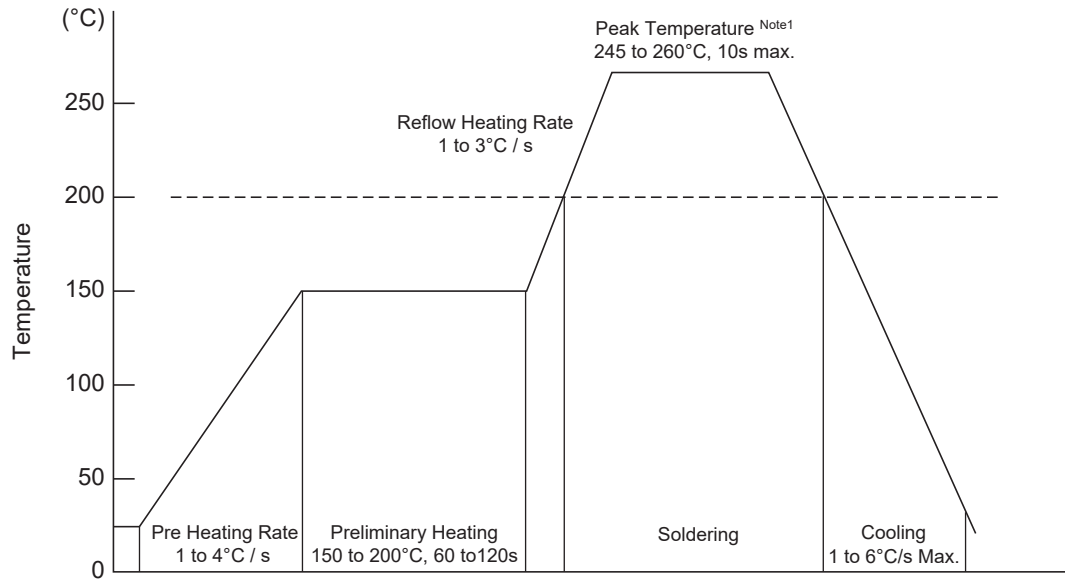
Note:

1. Package Body Sizes Exclude Mold Flash and Gate Burrs
2. Controlling Dimension: In millimeters
3. General Tolerance: $\pm 0.1\text{mm}$
4. The Pad Layout is for reference purposes only



Conditions of Soldering and Storage

◆ Recommended condition of Reflow Soldering(Pb-Free Solder)



Recommended peak temperature is over 245°C. If peak temperature is below 245°C, you may adjust the following parameters:

- Time length of peak temperature (longer)
- Time length of soldering (longer)
- Thickness of solder paste (thicker)

Note1:

Maximum thermal excursion allowed during the reflow assembly is as follow:

- Temperature: 255°C~260°C
- Duration at peak soak : 30 seconds
- Number of reflow: 3
- **Conditions of hand soldering** ^{Note2}

- Temperature: 320±10°C
- Time: 3s max.
- Times: one time

Note2: Not recommended for mass production, an engineering project, or re-work, it is allowed. It should be used with caution

● **Storage conditions**

● **Temperature**

5 to 30°C

● **Humidity**

≤ 60% RH

● **Floor Life**

168 Hours

● **Recommended period**

Five year after manufacturing(Depends on storage conditions)

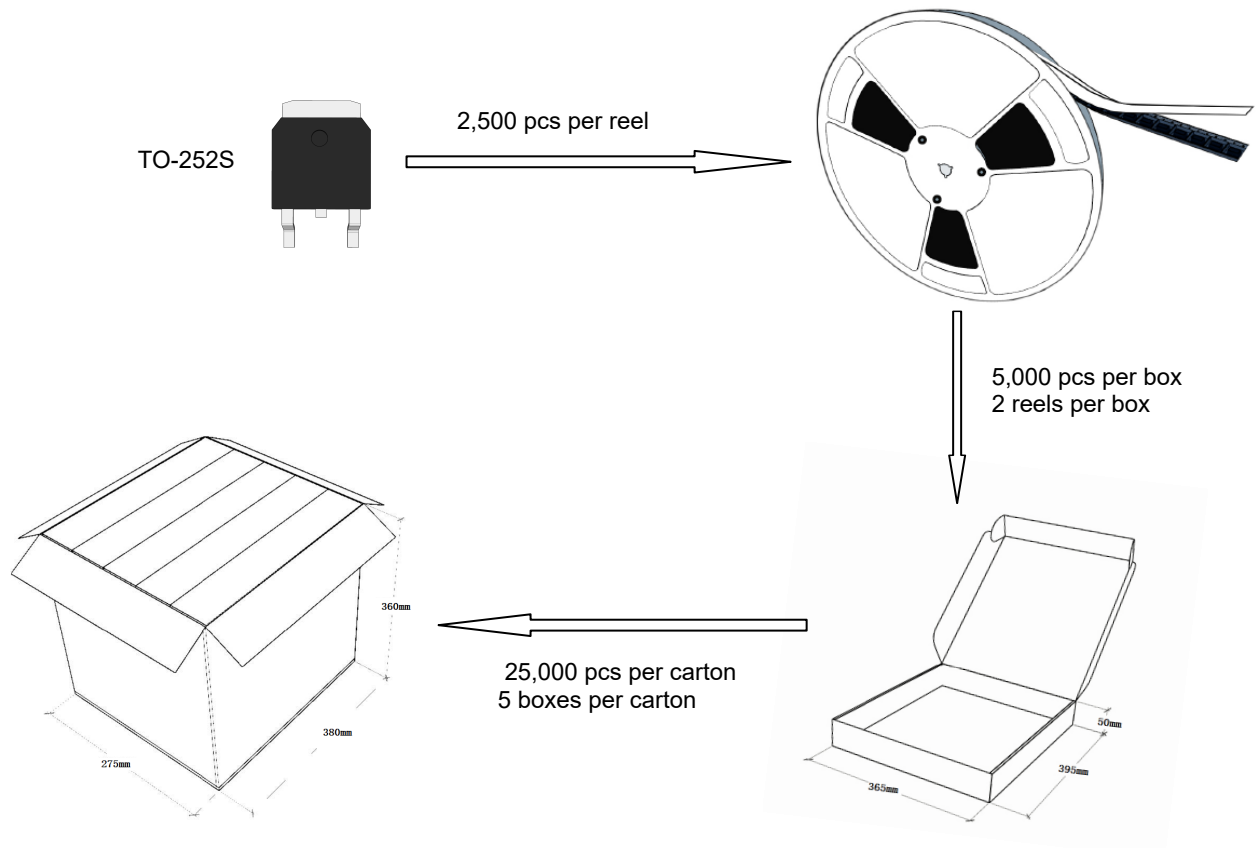


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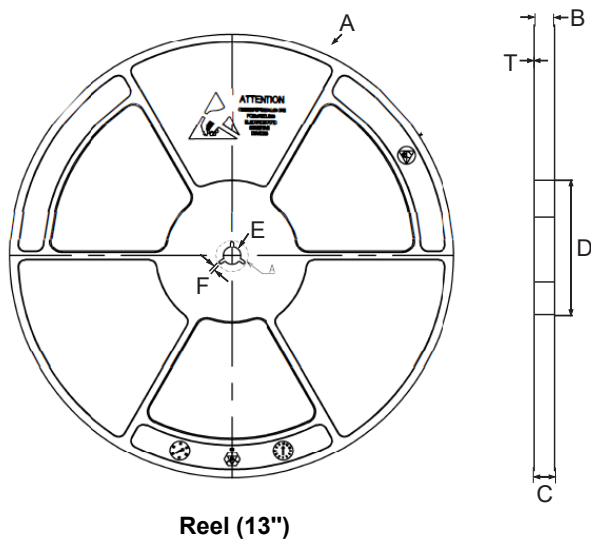
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Package Specifications

- The method of packaging



◆ reel data



Symbol	Value(unit:mm)
A	$\Phi 330.2 \pm 1$
B	17 ± 0.5
C	21.2 ± 2
D	$\Phi 100 \pm 0.5$
E	$\Phi 13.4 \pm 0.2$
F	2.3 ± 0.2
T	2.1 ± 0.2



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◆ Embossed tape data

